ABSTRACT

A semiconductor memory device including a memory cell block having a plurality of memory transistors formed on a semiconductor substrate. The memory transistors include first and second impurity-diffused regions and a gate formed therebetween. A plurality of memory cells are also included in the memory cell block and have lower electrodes connected to the first impurity-diffused regions, ferroelectric films formed on the lower electrodes and first upper electrodes formed on the ferroelectric films and connected to the second impurity-diffused regions. Further included are block selecting transistors formed on the semiconductor substrate and being connected to one end of the memory cell block. Second upper electrodes are also formed adjoined to the block selecting transistors and being disconnected from the first upper electrode of the memory cells.

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